A Study of CMOS VLSI Technology Landscape Challenges towards 7 nm

Kishore Prabhala
MSEE-Georgia Institute of Technology, USA, BSEE-Purdue University, USA-1981
Principal, PLNM Degree College, affiliated Acharya Nagarjuna Univsity since 2002
Director, VLSI Design Centre, PSK Research Foundation,
Opp. ANU Mens Hostel, Nagarjuna Nagar – 522 510, Guntur Dist., AP
9177408565, prabhalakishore@gmail.com

Abstract

CMOS VLSI design has grown in complexity from a million transistor to billion in last 20 years from 1 um critical dimension to 10 nm and IBM brings a successful 7nm IC. Billions of mobiles and tablets besides servers have been the major product developments that pushed CMOS Technology year by year as predicted Gordon Moore, founder of Intel in 1968. Commercial electronic products have impacted in many years of industry as well as consumers. As mobile landscape dramatically changing India, new products will developed with CMOS Technology Node complexity, Advanced Lithography Process and Scale of Economics of IC manufacturing. Hardware revolution in India will be driven to new heights with advent of IOT, Cloud Computing and Big Data Analytics. This paper reviews the key CMOS Technology parameters that have driven IC Designs from Fabrication to product developments that bring return on investment with lower risk.

Keywords: CMOS, Technology, Lithograph, Semiconductor, Integrated Circuits

Introduction

Mobile technology has been driven by CMOS VLSI design in areas such as microprocessor, memory, interface and radio frequency, RF and Wi-Fi circuits. Most of these circuits radically change with performance, power, area scaling, schedule, and cost (PPASC), a traditional matrix used chip makers, foundaries and system / product developers as technology node moving from 22nm to 14nm to 10nm to 7nm. Especially two products have been dominating as sales rose in billions in last three years and these are mobile phones and tablets. This hardware revolution would have much greater impact in developing countries for access of information and processing. A smart phone would be come first line server for common man in the growing era of cloud computing and big data analytics.

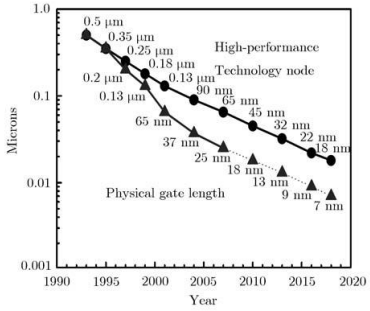
Conventional planar process of CMOS has been scaling down for last twenty years with faster circuit speed, higher transistor density and lower cost per transistor as defined by Gordon Moore of Intel. But there are great challenges encountered during the scaling which having been resolved by major firms as CMOS transistor size goes from 45nm to 22nm to 14nm to 10nm to 7nm [1][2]. Many Design firms moved out of Fabrication to concentration on product development as TSMC or Global Foundaries dominates manufacture while Nikon and ASML have brought newer machines for semiconductor fab. Apple has brought finest products such as iPad, iPhone, iPod, iTV with better IC designs. Only Samsung and Intel control their products in every aspect yet IBM has been working with fabrication firms to excel in newer technologies such as IOT, Cloud Computing and Big Data Analytics. Semiconductor market has out grown software sector worldwide in last five years.

Fabrication of CMOS integrated circuits of these sizes requires an accurate separation of logic and transistor design through layout into the multiple masks. There need to be precise mask alignment during lithography steps. There need be a greater control of many process variables such as gate length, metal line, dosage, oxide growth, etch, and overlay.

Technology Leap with Moor's Law

Gate length has been reduced as per Moore's law with 0.7 scaling factor 90nm to 65nm to 45nm to 32nm or 22nm. Intel had aggressively scale down the gate length from 90 nm to 45 nm, sometimes lower as shown in figure 1. But short channel effects led to the poly gate contact and metal pitch as technology node, but gate length may not reduced as much. FinFET has take this into another dimension with better electrostatics and higher drive current.

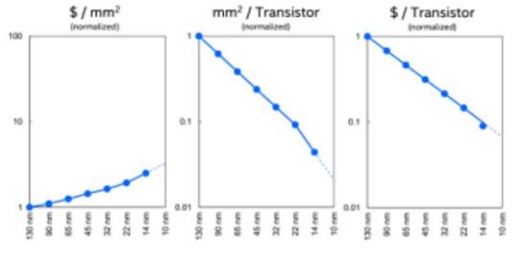
Figure 1: Technology vs Gate Length [3]



As shown in Figure 1, according to ITRS, CMOS technology has been used to develop 14 nm or 10 nm node at 2016 by adopting novel device structure, new lithography and new materials. The physical gate length and printed gate length of the device can be scaled down to 7 nm and 5 nm respectively [3]. IBM has been a leader of semiconductor technologies along with Intel, Samsung, Apple, AMD, TSMC, Global Foundaries, Toshiba, etc. Smallest 6T SRAM cell was designed by IBM with the area of only 0.128 μm^2 based on 22 nm technology. [4]

At ISSCC 2015, Intel had explained various parameters of 14nm as shown in figure 2. These are more transistors per mm but cost of the process technology will be increase at 10nm. One can see more transistors in the same area with improved performance and lower price per transistor

Figure 2: Intel Technology progress in 2015 [5]



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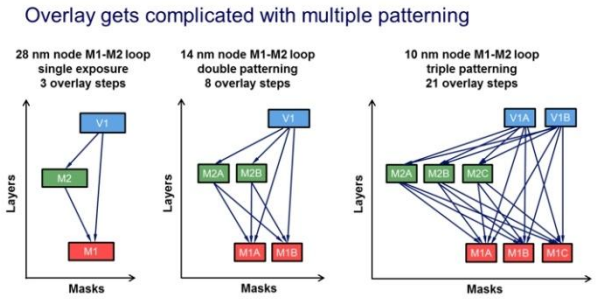
Lithography Advancements

Lithographic pitch scaling has been the key driver for CMOS technology in last five years as seen from figure 1. Semiconductor lithography has been stuck with 193 nm immersion (193i) lithography for over a decade. Double or triple pattern is a process technique allows any VLSI firm to use two or three masks for making a geometric pattern such as poly for gate or metal through contact or via. This is not possible with single exposure. This is very similar to a colour mixing of red, green and blue leads to many colour patterns in printing on paper. Merging patterns from few separate exposures is the key. These are complex steps and increase cost factor by order 4 or 8.

The litho-etch-litho-etch, (LELE) scheme is the one that has been explored for several years [6]. Critical dimension (CD) can be controlled with precision, Depth of Focus (DOF) is more accurate and lower cost for Design for Manufacturability, (DFM).

Figure 3. Multiple patterns in 90nm to 14nm technology [6]



Masking pattern define the cost of chip making and as technology node move to lower nano meter technology cost would be much higher and newer lithography process such as EUV or E-Beam must pave wave for cost reduction as shown in table 1.

Table 1: Mask Steps currently used in various Technology Nodes

Node	28 nm	20 nm	10 nm	7 nm immersion	7 nm EUV
Lithography Steps	6	8	23	34	9
Overlay Metrology	7	9-11	36-40	59-65	12

Cost Factor for technology implementation

A key technology change has been used for lithography to process 20 nm technology node to 5 nm technology node is EUV exposure tool besides double or triple patterning with high NA water-based immersion lithography. This uses a 13.5 nm extreme ultraviolet light and plain mirrors. The huge non-recurring expense to invest in 22 nm to 10 nm fabrication equipment and process development is expected to exceed 10 billion dollars, which is only possible at few semiconductor firms. This is shown in table 2. [7]

Table 2: Cost of Technology [7]

Technology Node	90 nm	65 nm	45 nm	22 nm
Fab Cost in billions of dollars	2.8	3.8	6.9	9.5
Process Development cost in $Billions	2.2	2.6	3.2	6.8

As shown in the above table the key parameters for billion transistor chip the cost of design of chip comes down as it penetrates with millions of devices just like a feature phone or a smart phone or a tablet. IC Design cost for a 10nm chip is $120 million but it is $271 million for a

7nm chip, according to Gartner. But a 14nm chip has a cost of $80 million as more firms releasing chips with and even more used 28nm planar device costs only $30 million.

Table 3: Key CMOS Technology Parameters

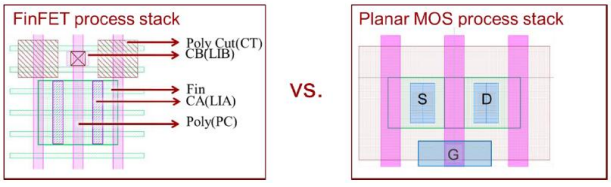
Technology	65 nm	45 nm	32 nm	22 nm	14 nm	10 nm
Year of Use	2005	2007	2009	2011	2013	2015
Device's	IBM FPGA	Xeon 5400 S	4i	Intel Core 7	iPhone 6s	TSMC
Frequency	1.8 GHz.	1.8 GHz	1.8 GHz.	1.8-3.0 GHz.	3.8 GHz	3.8 GHz More
Gate Length	35 nm	30 nm	25 nm	18 nm	12 nm	9 nm
Kgate /mm2	0.8	1.5	2.8	5.2	9.0	16.0

According to Gartner, only 100 engineer-years require to bring a 28nm IC which is more for a for 14nm design and the number is 200 engineer-years. Latest technologies have even more time needed for IC design. It is 300 engineer-years for 10 nm IC and 500 engineer-years for 7nm IC. So, at 7 nm, a group of 100 engineers needed for 5 years to complete IC design to tape out or may be 250 engineers for 2 years. This is a key issue for VLSI IC design.

FinFET as the latest technology driver

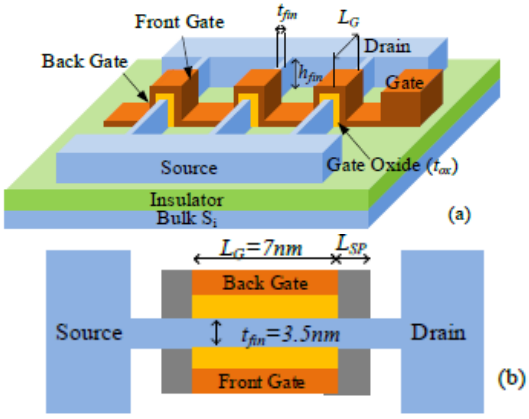
Planar CMOS has driven the semiconductor industry for more than three decades. Owing to excessive leakage and variation, the industry is moving from planar CMOS to FinFET below the 20 nm node. Figure 3 shows a 3-fin FinFET. FinFET has the gate covering the channel (fins) on more than one side, providing better gate control over the channel and higher performance. FinFETs are expected to scale to 7 nm node as presented by IBM in 2016.

Figure 4 FinFET with Planar MOS



The process stack of the FinFET device is shown in Figure 5 and compared with a planar CMOS process stack. [9]

Figure 5: FinFET device and Fab view



Conclusion

CMOS VLSI has been dominant technology in IC product development not only in defence electronic product development as well as consumer product development. But mobile technology will give business people, academia and students from India to make products that technically par excellancence. Design, Fabrication and Economics are three key areas as Indian engineering manpower leads in million across many states and hope entreprenues give them financial muscle for better innovative products based on 14 to 10 to 7 nm CMOS Technology

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