Performance Comparison of 64-Bit Adders

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***Abstract*— The objective of this paper is to analyze and optimization of adders. Addition is essential operation in any digital, analog and control systems. Adders are part of not only arithmetic logic unit in computers but used in some other kind of processors too, where they are used to calculate addresses, table in dices , and similar operations for that we have to reduce the area. This paper mainly concentrated on the optimization of the area. As number of bits increase to add, the area would be increased to calculate the carry from each section. In this paper, we implemented the adders using mentor graphics tool. Simulation have done by Questa_sim and synthesis by Leonardo spectrum in 135nm technology.**

***Keywords*— Questa_sim , Leonardo spectrum , mentor graphics, optimization, synthesis.**

I. INTRODUCTION (HEADING 1)

Adder is a basic and indispensable circuit for arithmetic operations in digital system. Careful design and analysis of adder is most important for the speedy and accurate function of overall electronic system. Arithmetic unit is the essential block of digital systems such as Digital Signal Processor (DSP), micro processors, micro controllers, and other data processing units. Adders become critical hardware unit for the efficient implementation of arithmetic unit. In many arithmetic applications and other kinds of applications, adders are not only in the arithmetic logic unit, but also in other parts of processor. Addition operation can also be used in complement operations (1's, 2's, and so on), encoding, decoding and so on. In general, addition is a process which involves two numbers which are added and carry will be generated. The addition operations will result in sum value and carry value. All complex adder architectures are constructed from its basic building blocks such as Half Adder (HA) and Full Adder (FA).

Addition is the basic operation of any digital system. An effective functioning of adder holds a role of major importance in the architecture of more complex structures such as arithmetic logic unit of microprocessors. Arithmetic calculations are covered under logical levels while the area and other factors are covered under circuit levels. In the next sections different architectures of different adders are discussed with the preference to area, number of components and speed of each device.

II. RIPPLE CARRY ADDER

RCA contains series structure of Full Adders (FA) as shown in figure 1; each adds two bits along with carry bit, but not at the least significant bit. The Generated carry from each full adder will be taken as input at the next full adder and so on. Hence, the carry is propagated in a serial computation or rippled. RCA is simple to design but consumes more delay since the carry bit of last full adder is valid only after the joint propagation delay of all full adder cascaded. Hence, delay is more as the number of bits is increased in a RCA.

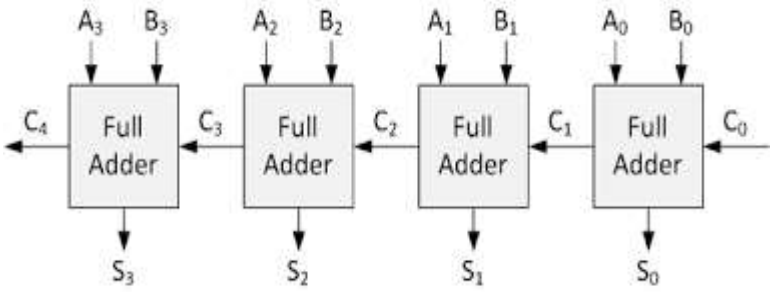

Figure-1: Ripple Carry Adder

III. CARRY LOOK AHEAD ADDER

Carry Look Ahead (CLA) design is based on the principle of looking at lower adder bits of argument and addend to generate carry at the higher order bits. This adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate. This adder brings two internal inputs known as "Generation" (G) and "Propagation" (P) at each stage. The generation values and propagation values are computed. Internal carry generation is calculated in second stage as shown in figure 2.

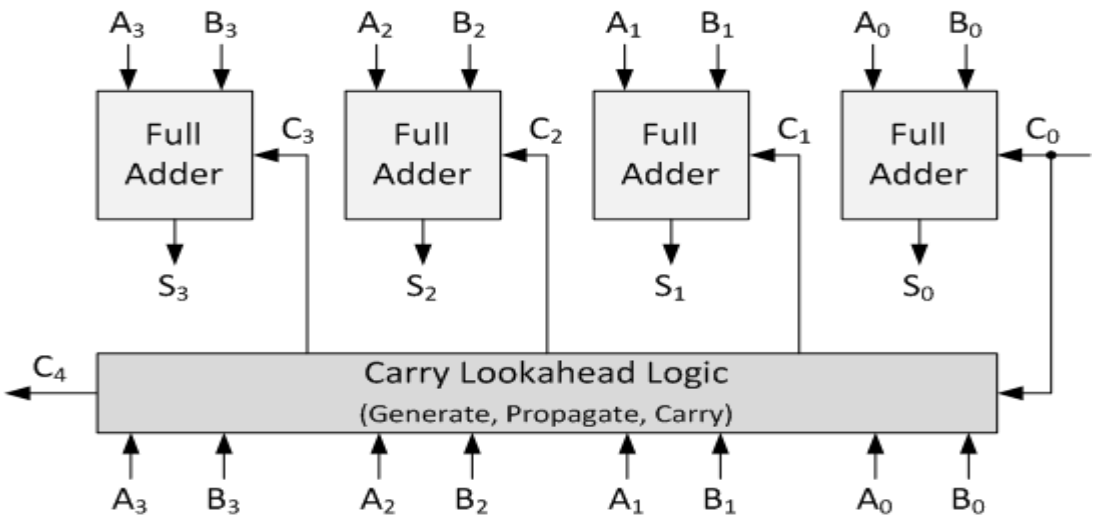

Figure-2: Carry Look Ahead Adder

IV. SIMULATION OF RCA AND CLA

Two types of adders designed were for 64 bit in Mentor tool called Questa_sim and Leonardo spectrum and these are RCA and CLA. The simulation with high level language scripts in Mentor was shown for RCA in figure 3 and CLA was shown in figure 4.

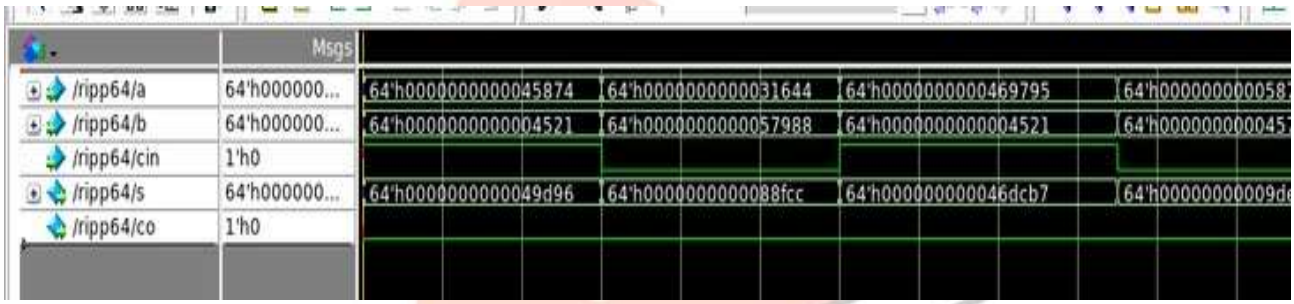

Figure 3. Simulation of Ripple Carry Adder

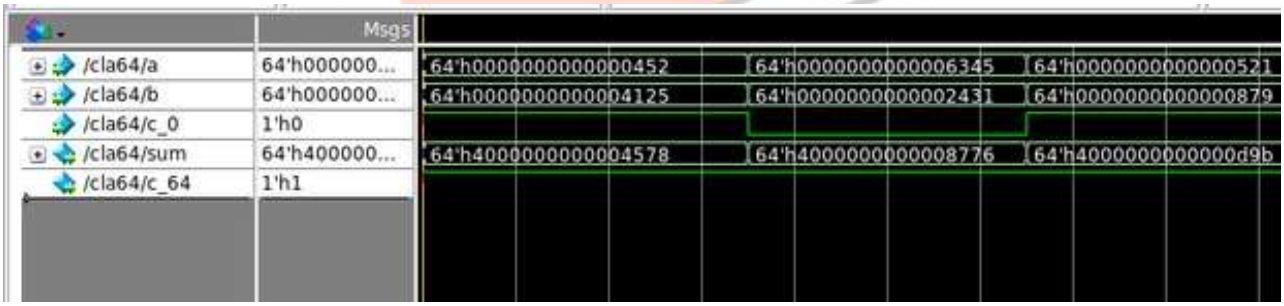

Figure 4. Simulation of Carry Look Ahead Adder

V. RESULT

The Ripple Carry Adder, Carry Look Ahead adders had been simulated for 64 bits using Mentor graphics with 135nm CMOS technology. The simulation results of these two adders are compared in terms of delay and area and shown in table 1. Gate count has been increased in CLA because at each adder stage Generate and Propagate logic has to be built which is less than 2 percent. But the delay got reduced by over 40 percent from 22 ns to 12.9 ns in this 64 bit design.

Table 1: Area and Delay comparison of RCA and CLA

NAME	GATE COUNT	DELAY
Ripple Carry Adder	5461	22.0 ns
Carry Look Ahead Adder	5574	12.9 ns

VI. CONCLUSION

New and fast algorithms are implemented at the cost of one or the other factors of delay or area or power as technology moving towards 45 to 22 nm. Ripple carry adder is the most basic adder used in arithmetic logic, just by joining adders with no exercise on speed reduction. Carry Look Ahead adder designed to reduce propagation delay, especially in carry. Though the most

efficient way to add n bits numbers is by the use of Kogge Stone adder in which the number is added bit by bit from LSB to MSB but moving to faster technologies interconnection of transistors becomes a dominant factors. Several architectures are often close to the optimum performance can be selected for the given design. The results show that the given methodologies lead to the best design if Electronic Design Automation tools are used at all technology nodes.

VII. REFERENCES

[1] Raminder Preet Pal Singh, Praveen Kumar, Balwinder Singh,"Performance Analysis of 32-Bit Array Multiplier with a Carry Save Adder and with a Carry Look Ahead Adder", Letters of International Journal of Recent Trends in Engineering, Vol. 2, No. 6, pp. 83-89,Nov 2009.

[2] G.Shyam Kishore,"A Novel Full Adder with High Speed Low Area",2nd National Conference on Information and Communication Technology (NCICT) 2011 Proceedings published in International Journal of Computer Applications® (IJCA).

[3] Pakkiraiah Chakali, Madhu Kumar Patnala , " Design of High Speed Kogge-Stone Based Carry Select Adder", International Journal of Emerging Science and Engineering (IJESE) ISSN: 2319–6378, Volume-1, Issue-4, February 2013.

[4] Rajender Kumar, Sandeep Dahiya SES, BPSMV, Khanpur Kalan, Gohana, Sonipat, Haryana, "Performance Analysis of Different Bit Carry Look Ahead Adder Using VHDL", Environment International Journal of Engineering Science and Innovative Technology (IJESIT) Volume 2, Issue 4, July 2013.

[5] Jagannath Samanta, Mousam Halder and Bishnu Prasad De, "Performance analysis of high speed low power carry-look ahead adder using different logic styles," International Journal of Soft Computing and Engineering (IJSCE), vol. 2, issue 6, pp. 330-336, Jan- 2013.

[6] S. Kao, R. Zlatanovici, and B. Nikolic, "A 240ps 64-bit carry-look ahead adder in 90 nm CMOS," in IEEE Int. Solid-State Circuits Conf.(ISSCC'06), San Francisco, CA, Feb. 2006.

[7] V. G. Oklobdzija, B. R. Zeeydel, H. Q. Dao, S. Mathew, andR.Krishnamurthy, "Comparison of high-performance VLSI adders in nsenergy-delay space," IEEE Tran VLSI Syst., vol. 13, no. 6, pp. 754–758, June 2005.

[8] H. Ling, "High-speed binary adder," IBM Journal of Research and Development, vol. 25, no. 3, pp. 156–166, March 1981.

[9] T. Han and D. A. Carlson, "Fast area-efficient VLSI adders," in Proc.8th IEEE Symp.Computer Arithmetic, Como, Italy, May 1987, pp.49–56.

[10] V. G. Oklobdzija, B. R. Zeydel, H. Q. Dao, S. Mathew, and R. Krishnamurthy, "Comparison of high-performance VLSI adders in energy-delay space," IEEE Trans. VLSI Syst., vol. 13, no. 6, pp. 754–758,Jun. 2005.