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An Implementation of 32 BIT CMOS Comparator in Mentor EDA Tools

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Abstract: Comparison can be done with voltage level or current level in a given system using analog circuit of operational amplifiers but as digital interface became a common aspect of various systems since 1990s. CMOS logic dominates in bit wise comparison in any digital system and plays a vital role on many devices like Arithmetic Logic Unit (ALU), Microprocessor, Error detection, Digital Signal Processing (DSP) and Communication devices when two numbers are equal or which one is greater. In this paper a CMOS 32- bit comparator has been designed using Mentor tools. Comparator has two inputs, A and B. It produces three outputs, namely X,Yand Z. When A equals B the output X goes High or "1" a major process of equality check in any digital system. When A is greater than B, the output Y is "1" and when A is less than B, the output Z is "1". Simulation and synthesis have performed using mentor graphics at 135nm technology.
Keywords: CMOS, Comparator, Mentor Tools, 135nm Technology.

I. Introduction

The digital comparator is key components in any digital system and used in many digital processes of computing and communication including sorting and searching data. It is heavily used in data intensive applications such as Image processing and graphics require millions of comparisons as technology of storage crossed Giga bytes and speed of microprocessor rose over a Giga Hertz. Searching for a data or sorting data requires a comparison two points of a data having width of a byte or more. Comparison of at each has to be done. A digital comparator need to be designed carefully to make any system fast and efficient.

Binary comparators or logical comparators use combinational logic circuits of Exclusive NOR, AND, OR and Inverter for three possible combinations equal to or greater than and less than between two values or words. Comparator is a basic arithmetic unit that checks two binary numbers with two inputs A and B, and produces two are three outputs. One output if A is greater than B or B is greater than A and also the output if A is equal to B. It is an important data-path element for any general purpose architecture as well as an essential device for application specific integrated circuits (ASIC) and signal processing architectures. Comparators are also used in sorting networks which play an important role in areas such as graphics, remote sensing, parallel computing, multi-access memories and multiprocessing.

As the speed of microprocessor racing from few Mega Hertz to over a Giga Hertz with memory of RAM has been over few GBs and storage has topped few Tera bytes high throughput rates are needed in any system and lower delay of comparison plays a vital role. So, high speed design of comparator using CMOS brings lower power feature too as research gathers momentum in this area. The serial architecture is suitable when the inputs have fewer bits. When 32 bit or 64 bit inputs need to be compared the delay path depends on lower bits just like in a ripple carry adders as each lower bit needed to be compared when higher bits are equal. The circuit complexity increases.

In Section II, the design of digital comparator has been described. The proposed architecture for a 32-bit digital CMOS comparator has been presented in Section III. Section IV contains coding, logic diagrams, and the simulation results and the comparison to previous literature. The conclusions have been given Section V.

II. Basic Comparator Design

The design of digital comparator has two inputs with two bits each three output bits. The output A=B goes high if all the bits of A are equal to the corresponding bits of B. There are two more output signals which tells when A > B and A < B. If Most Significant bit (MSB) of the two numbers are unequal, i.e when Ai=1, Bi =0 then A>B or Ai=0, Bi =1 for A<B. But it the MSB are equal, check the next lower bit and the process continues, i.e. $A_i=B_i$ and $A_{i-1} = 1$, $B_{i-1} = 0$ then A>B or $A_i=B_i$ and $A_{i-1} = 0$ $B_{i-1} = 1$ then A<B. [1]

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Table 1: Truth Table for 1 bit Comparison

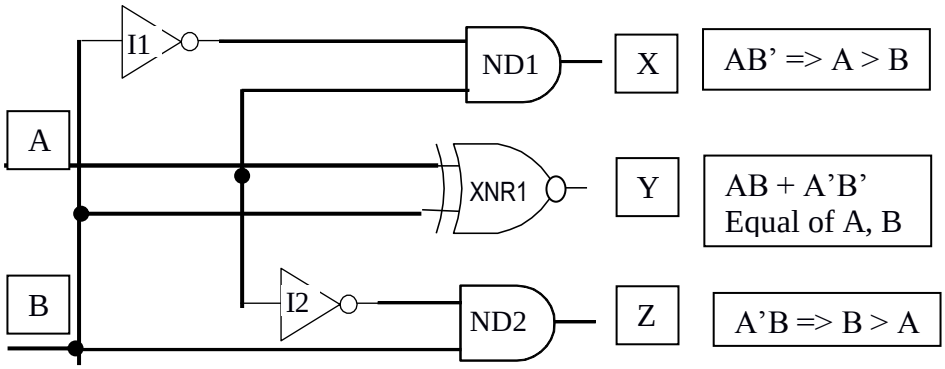
Input A	Input B	Output X Equal	Output Y A > B	Output Z A < B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

From the truth table one can easily find

X = A'B' + AB,
Y = AB'
Z = A'B

The logic for a 1 bit comparator is shown in Figure.1 Gate ND1 produces the output for the function A>B and ND2 produces the output from A<B while XNR1 is an XNOR gate giving an equality output. This basic circuit can be used to produce a comparator for any number of bits but more bits the circuit needed as comparison goes next level and becomes complex at four or eight bits.

Figure 1: Logic Diagram for 1 bit Comparator



A two bit input has four combinations logically and comparing with another 2 bit there are four comparisons though need the truth table has 16 entries. Similarly, a three bit inputs have eight comparisons, at each bit level from A0 with B0 to A7 to B7. At 4 bit there will be 16 times 16 binary patterns of inputs but simplification can be easily seen. The output for "Equality" will be done by a Exclusive NOR of each of the two bits at same position and all of them have to be AND for a final output of 1 if all are ZERO or ONE. For a 2-bit design needs two 2-input XNORs and a two input AND, for a 3-bit design needs three 2-input XNORs and a three input AND, and for a 4-bit design needs four 2-input XNORs and a four input AND. Delay increases slightly with 3 input AND and 4 input AND because there are n-MOS transistors in series. With an eight bit input, a design can be used with two layers of NANDs with two 4-input NANDs and a two 2-input NANDs to reduces the delay.

Figure 2: Truth Table for 2 bit input Comparison

A1	B1	A0	B0	A EQ B	A GT B	A LT B
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	1	0	0
0	1	x	x	0	0	1
1	0	x	x	0	1	0
1	1	0	0	1	0	0
1	1	0	1	0	0	1
1	1	1	0	0	1	0
1	1	1	1	1	0	0

From the truth table one write the equality as

$[A1 \odot B1].[A0 \odot B0]$ - 2.1

Input A greater than input B as

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A1.B1' + A0.B0'[A1⊙B1] - 2.2

Input B greater than input A as

A1'.B1 + A0'.B0[A1⊙B1] - 2,3

So the design begins with a XNOR of higher bit and if equal then compare lower two bits with higher equality for greater or lower logical condition. So, the n bit comparisons will have n-1 logic gates of XNOR as inputs to a NAND and this is the delay same as in a Ripple Carry Adder. As shown on equation 2.2 and 2.3 checking at bit 0 will be ANDed with equality at bit 1.

Table 2: Truth table of 4-Bit Digital Comparator

COMPARING INPUTS						OUTPUT
A_3, B_3	**A_2, B_2**	**A_1, B_1**	**A_0, B_0**	**A > B**	**A < B**	**A = B**
$A_3 > B_3$	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A1 < B_1$	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H
H = "1", L = "0", X = Don't Care						

For a four bit comparison of A with $A_3A_2A_1A_0$ and B with $B_3B_2B_1B_0$

A = B if $A_3=B_3$, $A_2=B_2$, $A_1=B_1$and $A_1=B_1$

Test each bit for equality with $X_i= A_iB_i+A_i'B_i'$ then equality is $(A=B) = X_3X_2X_1X_0$

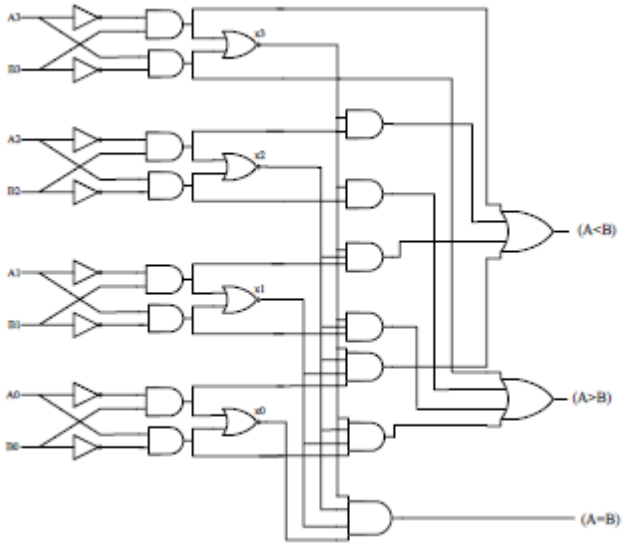
$$(A>B) = A_3B_3'+x_3A_2B_2'+x_3x_2A_1B_1'+x_3x_2x_1\,A_0B_0'$$
$$(A<B) = A_3'B_3+x_3A_2'B_2+x_3x_2A_1'B_1+x_3x_2x_1\,A_0'B_0$$

III. Logic Design with 4 bit Comparator

Logic for a 4 bit comparison is shown in figure 3 with comparing most significant bits from the top. $A_3'B_3$ from a AND and A_3B_3'+ from another AND feed a NOR get exclusive NOR. This feeds into a AND to get quality at the last four input AND.

A > B gets checked is at each stage and fed into a OR and similarly B > A too. This has been coded into a verilog model using Mentor tools and shown in figure 4.

Figure 3: Logic Diagram for a 4 bit Comparator



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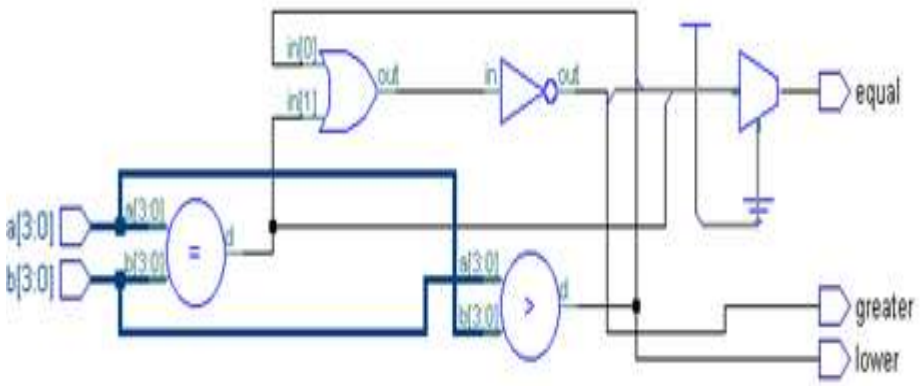
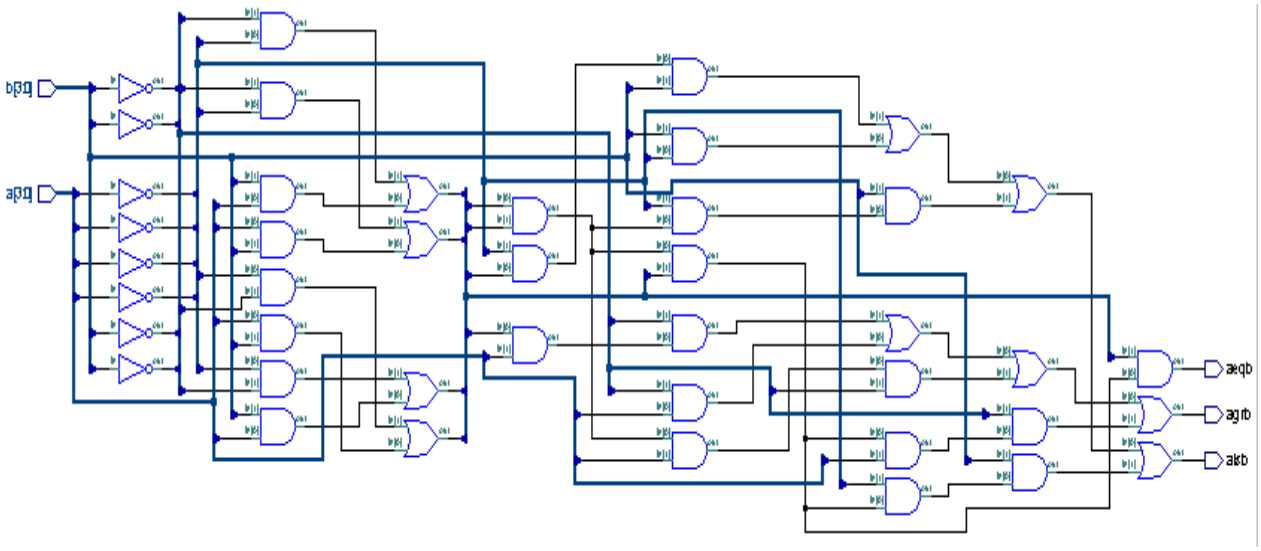
This has been coded into a verilog model using Mentor tools and shown in figure 4.

Figure 4: Verilog Model for a 4 bit Comparator



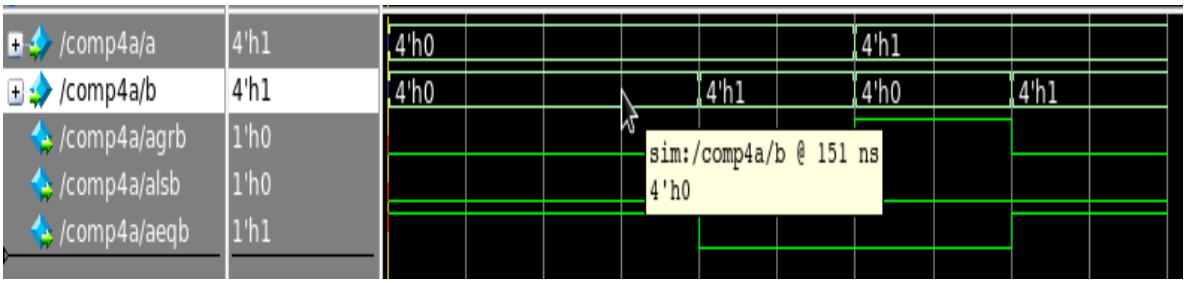
As logic synthesis has been done in Mentor, a logic model appears as shown in figure 5 and will be simulated for correct results.

Figure 5: 4 bit comparator from Verilog Code in Mentor tools



A simulation of the logic shown in figure 6 has been tested for an input A = 0, B = 0, Output Equal at the bottom of the figure was high. Next B = 1, then second output A < B (alsb) went high and when B = 0 and A = 1 A > B went high (agrb). Againg when B = 1, Equality went high.

Figure 6: 4 bit comparator from Verilog Code in Mentor tools

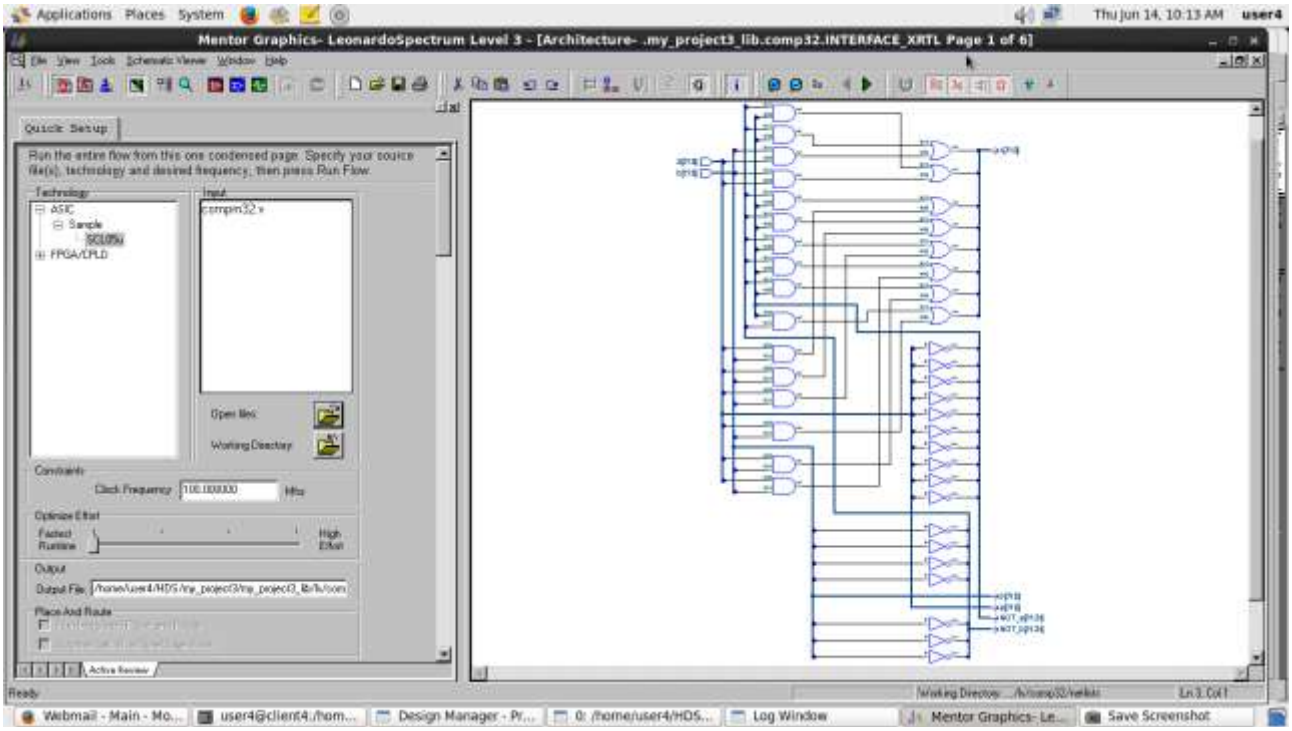


IV. Logic Design of 32 Comparator

Using the 4 bit logic defined earlier, a 32 bit comparator has been coded in the Mentor EDA tools and the logic diagram has been generated as shown in figure 7. The idea of 32 comparator has long path delay and it is to deter mine A > B. IF A31=B31, then check A30 with B30 and so on with 31 comparisons with a XNOR, all are feeding a AND then top if A0 > B0 then A will be bigger than B. Same for B > A. This delay can be less with technology

moving from 90nm or 65nm or 45nm.

Figure 7: Logic diagram for a 32 bit comparator from Verilog Code in Mentor tools



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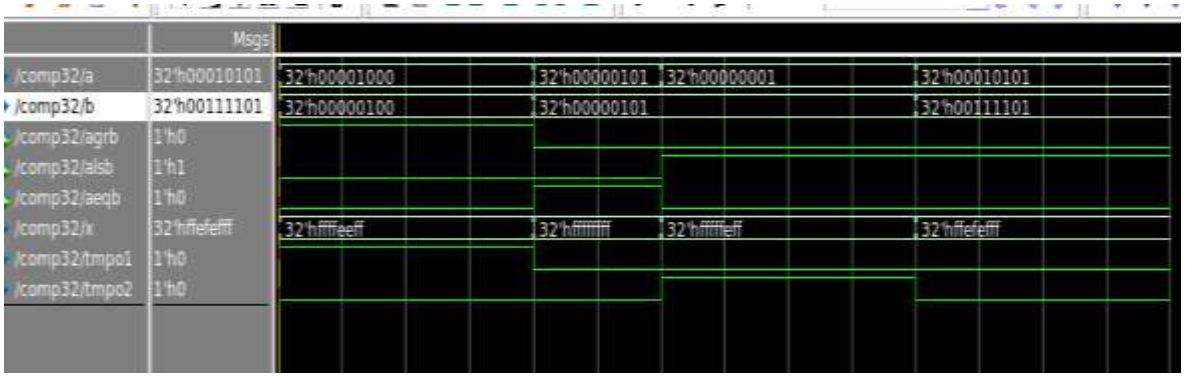
A simulation of the logic shown in figure 8 has been tested for an input A = 8, B = 4, Output A> B went high (agrb). Equal at the bottom of the figure was high when A = 101 or 5 and B is same. Next A = 1, then the output A < B (alsb) went high and when A = 10101 (21) and B = 111101, A < B still on high (alsb).

Figure 8: 4 bit comparator from Verilog Code in Mentor tools



V. Results and Conclusions

Table 3 shows the number gates used in the 32 bit CMOS comparator with 1358 logic gates and with delay of 9.94ns for 32 bit comparator design.

Table 3. Simulation Results of 32 bit comparator, gates and delay

Parameter	Value
Logic Gates	1358
Delay	9.94ns

Conclusion

Proposed comparator has been implement in Mentor EDA tools and simulated for functional verification and delay analysis of data from most significant bit to least significant bit. Being functionally correct, it is envisaged that the proposed architecture can be use in many applications of digital systems. A critical path need to be explored when A0 compares with B0, if there are 31 equal comparisons from A31 to B31 leading A1 to B1, a key concept will be explored. In this case A0 < B0 then A < B, else A > B.

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